G S NITESH NARAYANA

Barcelona ◇ Spain
(+34) 66401-2293 · (+91) 88859-55255 ◇ email@nitesh.contact ◇ nitesh.contact

VISION

To work in world-class research labs, solving challenging real-world problems using computer architecture.
Current Requirements

Actively seeking an internship opportunity within industry research teams focused on, but not limited to, general-purpose and vector micro-architectures, as well as H/W-S/W Co-Design for specialized workloads.

EDUCATION

Universitat Politècnica de Catalunya- UPC Barcelona *2021-Present*
PhD in Computer Architecture, ERC Grant CoCo-Unit
Advised by: Prof. Antonio González

Indian Institute of Information Technology Design and Manufacturing Kancheepuram, Tamil Nadu, India *2016-2021*

B.Tech in Computer Engineering + M.Tech in Computer Engineering
CGPA 9.22 (with Distinction, Ranked among Top 5 in class)

Delhi Public School Hyderabad *2003-2016*

Class 10 CGPA: 10/10

Class 12 Percentage: 93.2

PUBLICATIONS

1. **Nitesh Narayana GS**, Marc Ordoñez, Lokananda Hari, Franyell Silfa, and Antonio González. "ReuseSense: With Great Reuse Comes Greater Efficiency; Effectively Employing Computation Reuse on General-Purpose CPUs". In: *arXiv preprint arXiv:2311.10487*. 2023
2. **Nitesh Narayana GS**, Franyell Silfa, and Antonio González. "Characterizing DNN Workloads on General Purpose CPUs". In: *ACACES 2022: Poster Abstracts*. 2022, pp. 27–31

EXPERIENCE

Research Assistant October 2021 - Present
PDI, ARCO Research Group *UPC Barcelona - Barcelona, Spain*

· Implemented ARM SVE instructions for official gem5 main repo (to be merged in next release)
· Enhancing performance and energy efficiency of general-purpose CPUs for specialized workloads, with emphasis on vector units.
· Conducted in-depth analysis and characterization of Cognitive workloads with a focus on ARM SVE vector extension support. Developed workloads utilizing ARM-NN and Compute Library.

- Designed and implemented vector extensions and special units for ARM CPUs, contributing to the advancement of processor capabilities.
- Mentored and supervised a Bachelor's student in Computer Science, providing guidance and support throughout their research project.

Research Intern June 2021 - August 2021
Researcher, CAIRN/TARAN Team *IRISA - INRIA, Rennes - Bretagne Atlantique, France*

- Worked on design space exploration for LSTM accelerators on FPGA/DPU using Vitis AI / HLS frameworks.

Co-Op Engineer August 2020 - July 2021
Core Performance Team *AMD, India Private Limited, Bangalore*

- Designed a fast simulation paradigm for AMD's in-house cycle accurate core simulator, enhancing the efficiency of simulation processes.
- Conducted workload characterization to extract cacheline-level information for value prediction and identified potential optimizations.
- Developed a comprehensive verification environment and strategies for AMD's next-generation cache organization, ensuring the robustness and effectiveness of the design.
- Benchmarked and compared GPU performance under machine learning workloads, providing valuable insights for performance optimization and decision-making.

Research Intern July 2019 - July 2021
Researcher *IIT, Madras*

- Collaborated with Prof. Madhumutyam to tackle challenges related to Prefetching in SSDs and Value Prediction, contributing to advancements in performance.
- Developed a simulator for Deep Learning Accelerator as part of a project supervised by Prof. Pratyush Kumar at RISE Labs
- Conducted research on DRAMs, memory devices, and controllers, exploring topics such as refresh rates and data persistence using FPGAs. Utilized various simulators to analyze and understand different metrics under the guidance of Prof. V. Kamakoti and Prof. Chester Rebeiro.

Project Intern @ Shakti Team RISE Labs May 2019 - July 2019
Researcher *IIT, Madras*

- Designed DUT interface integrated with Spike simulator for Verification of Shakti RISC-V Processor. Worked on other RISC-V based simulators.

Research Assistant @ HPRCSE Lab December 2018 - July 2020
Researcher and Lab Incharge *IIITDM, Kancheepuram*

- Conducted research on various topics in Computer Organization & Architecture and Network Systems, including Circuit Obfuscation, Branch Prediction, and Hardware Packet Classification.
- Mentored student projects, providing guidance and support for research and development.
- Served as a resource person for lab workshops, sharing expertise to enhance participants' understanding of relevant topics.
- Managed and supervised winter break interns, fostering their professional growth and aligning their contributions with project objectives.

CavinTek, Sand-Box Program December 2017 - January 2018
GUI Developer *MadeIT, IIITDM Kancheepuram*

- Project: Automated Physical File Tracking System for CavinTek under MadeIT
- Headed the design and development of the Software Design team for the project. Developed the API in Visual Studio with SQL Server as the back-end.

TALKS

Design Thinking and Thinking Design Workshop September 2019
Resource Person and Organizer *Delhi Public School, Hyderabad*

· Conducted a workshop, for class XI Students, dealt with shining light on unorthodox thinking methodologies for solving real world problems.

High Performance Computing Workshop by HPRCSE December 2018,2019
Resource Person *IIITDM, Kancheepuram*

· Annually conduct workshop on HPC, give lectures on Code Profiling(GProf, LIKWID, Valgrind,Intel VTune) and CUDA programming, Nvidia architectures.

TEACHING EXPERIENCE

Advanced Computer Organization and Architecture Lab Fall 2019, 2020, 2022
TA/LA *IIT, Madras*

· Served as a teaching assistant for the course Advanced Computer Organization and Architecture with Lab under Dr. Madhumutyam(Professor of Computer Science Department, PACE Labs). Assisted students in understanding concepts related to ARM, x86, and RISC-V assembly, covering multiple versions of the course.

Computational Engineering LAB January 2018 - April 2018
TA/LA *IIITDM, Kancheepuram*

· Worked as the LAB Assistant during SEM-4 under Dr.N.Sadagopan (Assistant Professor of Computer Science and HOD).

CERTIFICATES AND GRANTS

DATE 2024 March 2024
Young Peoples Program Full Grant *Valencia, Spain*

ACACES HIPEAC Summer School 2022 June 2022
Attendance Grant *Fuigi, Italy*

CoDS COMAD 2020 Jan 2020
Attendance and Travel Grant *Hyderabad, India*

Foundations to Computer Systems Design NPTEL Course 2018-2019
All India Rank 1 *India*

POSITIONS OF RESPONSIBILITY

ISCA 2024 April 2024
PC Member (Artifact Evaluation)

HPCA 2024 November 2023
PC Member (Artifact Evaluation)

RISC-V Summit June 2023
Organizing Volunteer *Barcelona, Spain*

MATEO 2022 Workshop August 2022
Organizing Volunteer *BSC Barcelona, Spain*

CS Club January 2019 - June 2020
Head Core(since August) & Resource Person *IIITDM, Kancheepuram*

TECHNICAL STRENGTHS

Programming Languages	ARM Assembly, C/C++, Python, Verilog, x86
Tools & Packages	gem5, ARM-NN and Compute Library, McPat, Cacti, Vitis HLS and AI, Pytorch, TensorFlow, CoCoTB, AutoCAD

INTERESTS

Research Interests	Computer Hardware, Memory Systems, Domain Specific Architectures, Parallel Computer Architecture, Re-configurable Computing
Others	Design Thinking, Problem Solving, Teaching, Writing, Poetry Physics and Biology, Space Science, Music, Sketching Quantum Computation and Exploring New Domains

COURSES

Core

Computer Architecture, Computer Organization, Operating Systems, VLSI Design, Data Structures and Algorithms, Digital and Analog Circuits Design, Computer Networks, Automata and Compiler Design, High Performance Computing

Electives, Design and Other Courses

Systems Engineering for Deep Learning, Foundations of Computer Systems Design, Systems Thinking for Design, Intelligent Systems Design, Sociology of Design, Computer Vision

LANGUAGES

Expert	English, Telugu, Hindi
Learner	Spanish, Tamil

REFERENCES

Will be shared upon request